Description

[RAIL TO RAIL DUAL SLOPE ADC]

BACKGROUND OF INVENTION

[0001]   Field of the Invention

[0002]   This invention generally relates to a dual slope analog to digital converter, and more particularly to a dual slope analog to digital converter providing rail to rail input voltage range and finer resolution.

[0003]   Description of Related Art

[0004]   A conventional dual slope analog to digital converter (ADC) is illustrated in *FIG. 1*. According to the circuit, the input voltage range is narrow. For example, in the case that the input transistor pair of the input operational amplifier (OPAMP) *301* is NMOS, the input range of the OPAMP is from about 1V to VDD. In the case of the mobile application product or LSI using advanced process technology, the power supply voltage VDD is usually low, ranging from 1.5V to 3V. This makes the range of input voltage narrow, causing it difficult to get enough resolution of ADC. Thus

a dual slope ADC with rail to rail (VSS to VDD) input range
is desired.

SUMMARY OF INVENTION

[0005] An object of the present invention is to provide rail to rail
input range, a minor error and finer resolution of ADC.

[0006] Another object of the present invention is to provide a
dual slope ADC with a single pin external capacitor con-
nection.

[0007] The dual slope ADC circuit scheme of this present inven-
tion includes an input stage, an integrator stage, and a
comparator stage. For the input stage, the circuit is com-
posed of a first operational amplifier (OPAMP). The input
voltage is stored in a first capacitor, which is connected in
negative feedback loop fashion of the first OPAMP, and
this voltage is then applied between the output terminal
and the negative input of the first OPAMP. The first
OPAMP keeps the voltage of the positive input to be the
same as the negative input of which. The current flowing
through a first resistor is linearly proportional to the input
voltage, where the first resistor couples the output of the
first OPAMP and a second OPAMP, which is part of the in-
tegrator. The second OPAMP and a second capacitor work
as an integrator to charge the current from the resistor,

where the second capacitor is connected in negative feed-back loop fashion of the second OPAMP. The comparator stage, comprising a third OPAMP, checks the voltage across the second capacitor. A third capacitor coupling to the negative input terminal of the second OPAMP compensates the offset voltages of the first OPAMP. On the other hand, a plurality of switches are controlled to make the necessary connections for the different operation phases, including offset cancellation phase, integration phase, discharge phase, and charge reset phase. The phases are described as follows.

[0008] The offset cancellation phase of the rail to rail dual slope ADC of this present invention is described herein. At a stable state, the voltage across the first resistor becomes zero, the voltage across the third capacitor is equal to the offset voltage of the first OPAMP, the negative input of the second OPAMP is determined by an analog ground voltage (AGND) and the offset voltage of the second OPAMP, and the positive input of the third OPAMP is determined by the output voltage and the offset voltage of the third OPAMP.

[0009] The integration phase of the rail to rail dual slope ADC of this present invention is described herein. The voltage across the first resistor is the input voltage VIN. The cur-

rent through the first resistor charges the second capacitor and the output voltage of the second OPAMP decrease constantly if VIN is positive.

[0010] The discharge phase of the rail to rail dual slope ADC of this present invention is described herein. The voltage across the first resistor is the input voltage Vref, which is a predetermined constant voltage. The current through the first resistor discharges the second capacitor and the output voltage of the second OPAMP increase constantly if Vref is minus. The output voltage of the third OPAMP changes from low to high, when the output voltage of the second OPAMP across the initial voltage, which is determined after the offset cancellation phase. This change of the output voltage of the third OPAMP indicates the completion of the discharge phase.

[0011] The charge reset phase of the rail to rail dual slope ADC of this present invention is described herein. In this phase, unnecessary residual charge in the second capacitor is discharged to the initial voltage,which is determined after the offset cancellation phase. The difference from the offset cancellation phase is that the charge reset phase can discharge the unnecessary charge in the second capacitor more quickly than the offset cancellation phase.

Although the charge reset phase has the similar function as the offset cancellation phase, the offset cancellation is still necessary to refresh the voltage across the third capacitor.

[0012] Accordingly, the present invention has wider input voltage range than the conventional scheme, since the input voltage range of the present invention is rail to rail (from VSS to VDD) whereas that of the conventional scheme is about from 1V to VDD. For example, if VDD is 1.5V, the input voltage range of the conventional scheme is only 0.5V, while the input voltage range of the present invention is 1.5V, which consequently is able to provide finer resolution of ADC.

[0013] Moreover, since the input voltage of the first OPAMP is kept around AGND, the offset voltage of the first OPAMP is not affected by the input voltage, and a minor error and finer resolution are obtained in this present invention.

[0014] A simplified scheme of the rail to rail dual slope ADC of this present invention is described herein. In this configuration, there is no integrator OPAMP. Instead, the current flowing through the first resistor charges an external capacitor through single pin. The operation of the circuit is similar to that with integrator. The difference is that the

voltage of the positive input of the first OPAMP changes according to the terminal voltage of the external capacitor in the integration phase and the discharge phase. This change of the positive input of the first OPAMP reduces the input voltage range. Since the circuit is configured with single pin capacitor connection, this circuit is exemplary useful for applications that do not require high resolution but requiretemptemp small pin count and simple circuit. Notice that this circuit is applied to a VCO as an example.

[0015] The above is a brief description of some deficiencies in the prior art and advantages of the present invention. Other features, advantages and embodiments of the invention will be apparent to those skilled in the art from the following description, accompanying drawings and appended claims.

BRIEF DESCRIPTION OF DRAWINGS

[0016] *FIG.1* is circuit diagram illustrating a dual slope ADC according to a prior art..

[0017] *FIG. 2* is a circuit diagram illustrating a dual slope ADC according to the first preferred embodiment of the present invention.

[0018] *FIG. 3* is a circuit diagram illustrating a dual slope ADC ac-

cording to the first preferred embodiment of the present invention during offset cancellation phase.

[0019] *FIG. 4* is a circuit diagram illustrating a dual slope ADC according to the first preferred embodiment of the present invention during integration phase.

[0020] *FIG. 5* is a circuit diagram illustrating a dual slope ADC according to the first preferred embodiment of the present invention during discharge phase.

[0021] *FIG. 6* is a circuit diagram illustrating a dual slope ADC according to the first preferred embodiment of the present invention during charge reset phase.

[0022] *FIG. 7* is a circuit diagram illustrating a dual slope ADC according to the second preferred embodiment of the present invention.

[0023] *FIG. 8* is a circuit diagram illustrating a dual slope ADC according to the second preferred embodiment of the present invention during offset cancellation phase.

[0024] *FIG. 9* is a circuit diagram illustrating a dual slope ADC according to the second preferred embodiment of the present invention during integration phase.

[0025] *FIG. 10* is a circuit diagram illustrating a dual slope ADC according to the second preferred embodiment of the present invention during discharge phase.

[0026]   *FIG. 11* is a circuit diagram illustrating a dual slope ADC according to the second preferred embodiment of the present invention during charge reset phase.

DETAILED DESCRIPTION

[0027]   Reerring to *FIG. 2*, it is a circuit diagram illustrating a pre-ferred embodiment of this present invention. The input voltage VIN is stored in the capacitor *112*, and this voltage is then applied between the output terminal and the neg-ative input of the operational amplifier (OPAMP) *103*. The OPAMP *103* keeps the voltage of the positive input to be the same as the negative input of OPAMP *103*. The current flowing through the resistor *101* is linearly proportional to the input voltage. The OPAMP *106* and the capacitor *102* work as an integrator to charge the current from the re-sistor. The OPAMP *107* checks the voltage across the ca-pacitor *102*. The capacitor *105* compensates the offset voltages of the OPAMP *103*. Switches *104, 108, 109, 110, 111, 113*, and *114* are controlled to make the necessary connections for the different operation phases, including offset cancellation phase, integration phase, discharge phase, and charge reset phase. The circuits illustrating each the foregoing phases are shown in *FIGs. 3, 4, 5*, and *6* respectively.

[0028] Referring to *FIG. 3*, the offset cancellation phase of the preferred embodiment is shown therein. At a stable state, the voltage across the resistor becomes zero, the voltage across the capacitor *105* is equal to the offset voltage of the OPAMP *103*, the negative input of the OPAMP *106* is determined by AGND and the offset of OPAMP *106*, and the positive input of the OPAMP *107* is determined by the output voltage and the offset of the OPAMP *107*.

[0029] Referring to *FIG. 4*, the integration phase of the preferred embodiment is shown therein. The voltage across the resistor *101* is the input voltage VIN. The current through the resistor *101* charges the capacitor *102* and the output voltage of the OPAMP *106* decrease constantly if VIN is positive.

[0030] Referring to *FIG. 5*, the discharge phase of the preferred embodiment is shown therein. The voltage across the capacitor*112* is the input voltage Vref, which is a predetermined constant voltage. The current through the resistor *101* discharges the capacitor *102*, and the output voltage of the OPAMP *106* increase constantly if Vref is negative. The output voltage of the comparator *107* changes from low to high, when the output voltage of the OPAMP *106* across the initial voltage, which is determined after the

offset cancellation phase. This change of the output voltage of the comparator *107* indicates the completion of the discharge phase.

[0031] Referring to *FIG. 6*, the charge reset phase of the preferred embodiment is shown therein. In this phase, unnecessary residual charge in the capacitor *102* is discharged to the initial voltage, which is determined after the offset cancellation phase. The difference from the offset cancellation phase is that the charge reset phase can discharge the unnecessary charge of the capacitor *102* more quickly than the offset cancellation phase. Although the charge reset phase has the similar function as the offset cancellation phase, the offset cancellation is still necessary to refresh the voltage across the capacitor *105*.

[0032] Accordingly, the present invention has wider input voltage range than the conventional scheme, since the input voltage range of the present invention is rail to rail (from VSS to VDD) , whereas that of the conventional scheme is about from 1V to VDD. For example, if VDD is 1.5V, the input voltage range of the conventional scheme is only 0.5V, while the input voltage range of the present invention is 1.5V, which consequently is able to provide finer resolution of ADC.

[0033] Moreover, since the input voltage of the input OPAMP is kept around AGND, the offset of the OPAMP is not affected by the input voltage, and a minor error and finer resolution are obtained in this present invention. Whereas the scheme of the conventional circuit results in error for OPAMP *301* in *FIG. 1* is a voltage follower whose offset voltage changes according to the input voltage.

[0034] Referring to *FIG. 7*, it is a circuit diagram illustrating another preferred embodiment of the present invention. In this configuration, there is no integrator OPAMP. Instead, the current flowing through the resistor *201* charges the external capacitor *202*through single pin. The operation of the circuit of *FIG. 7* is similar to that of *FIG. 2*. The difference is that the voltage of the positive input of the OPAMP *203* changes according to the change of the terminal voltage of the external capacitor *202* in the integration phase and the discharge phase. This change of the positive input of the OPAMP *203* reduces the input voltage range. Since the circuit is configured with single pin capacitor connection, this circuit is exemplary useful for such applications that do not require high resolution but require small pin count and simple circuit. Notice that this circuit is applied to a VCO as an example. Also notice that the offset can-

cellation phase, integration phase, discharge phase, and charge reset phase are illustrated in *FIGs. 8–11* similarly to *FIGs. 3–6.*

[0035] The above description provides a full and complete description of the preferred embodiments of the present invention. Various modifications, alternate construction, and equivalent may be made by those skilled in the art without changing the scope or spirit of the invention. Accordingly, the above description and illustrations should not be construed as limiting the scope of the invention which is defined by the following claims.